Product Specification

Product Transparent Panel Kit

Model No. LCD-315-TRN

1.1 General Information

Item	Specification	Unit	Note
Active Area	697.6845 (H) x 392.2560 (V)	mm	
Cell Size	714.835(H) x 410.570 (V) x 1.900 (D)	mm	
Weight	1.2	kg	Max.
Driving Scheme	a-Si TFT Active Matrix	-	
Number of Pixels	1366 x 768	pixel	
Pixel Pitch (Sub Pixel)	0.17025 (H) x 0.51075 (V)	mm	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	16.7 M	color	8-bit
Display Mode	Transmissive Mode, Normally Black	-	
Glass thickness (Array/CF)	0.7/0.7	mm	
Color Chromaticity	R=0.638, 0.335 G=0.323, 0.621 B=0.156, 0.054 W=0.280, 0.290		Typical value measured at CSOT's module: MT3151A04-1
Contrast Ratio	4000:1(Typ.)		
Cell Transmittance	6.75%(Typ.)	%	
View Angle(CR>10)	+89/-89(H),+89/-89(V) (Typ.)		
Polarizer(CF side)	Anti-glare, Haze 12%, Hard Coating (3H)		
Polarizer(TFT side)	Hard Coating (3H)		

2. Electrical Specification

2.1 Open cell Power Consumption (TA = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	3	A	(2)
Power Supply Current	White Pattern	I_{CC}	-	0.30	0.36	A	(3)
	Horizontal Stripe	I_{CC}	-	0.27	0.32	A	
	Black Pattern	I_{CC}	-	0.18	0.21	A	

Note:

(1) The ripple voltage should be controlled less than 10% of V_{CC}.

(2) Measurement condition: V_{CC} rising time = 470 μs.

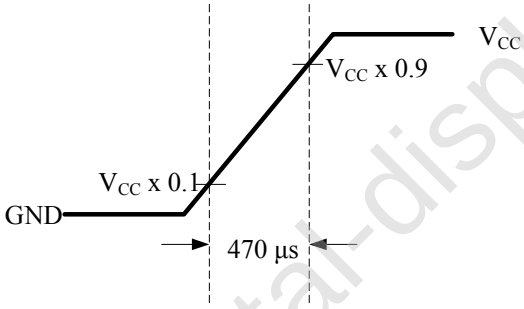
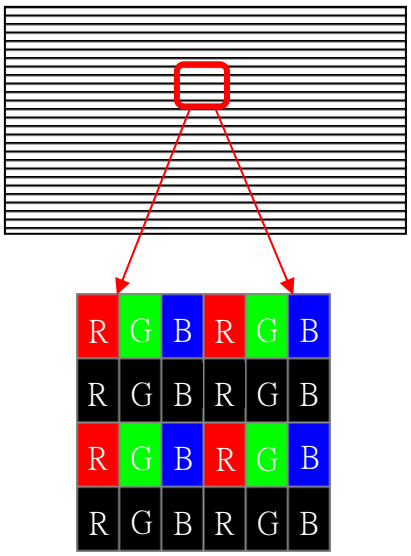


Fig. 2.1 V_{CC} rising time condition

(3) Measurement condition: V_{CC} = 12 V, Ta = 25 ± 2 °C, F = 60 Hz. The test patterns are shown as below.

A. White Pattern

B. Horizontal Pattern



C. Black Pattern

Fig. 2.2 Test patterns

2.2 LVDS Characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS Interface	Differential Input High Threshold Voltage	V_{TH}	+ 100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-	-	- 100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential Input Voltage	$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS Interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0.0	-	0.6	V	

Note:

(1) The LVDS input signal has been defined as follows:

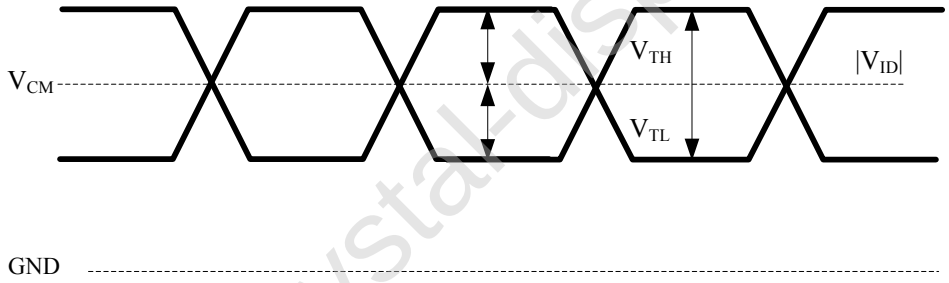


Fig. 2.3 LVDS input signal

3. Input Terminal Pin Assignment

3.1 Interface pin assignment

CN1: 300B30-0000RA-M4 (STARCONN) or equivalent (see Note (1))

Pin No.	Symbol	Description	Note
1	V_{CC}	Power Supply ,+ 12 V DC Regulated	
2	V_{CC}	Power Supply ,+ 12 V DC Regulated	
3	V_{CC}	Power Supply ,+ 12 V DC Regulated	
4	V_{CC}	Power Supply ,+ 12 V DC Regulated	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	LVDS SEL	LVDS Data Format Selection	(2)
10	NC	For CSOT Users Only	
11	GND	Ground	
12	LV1N0	1st Channel LVDS Data Input (0-)	
13	LV1P0	1st Channel LVDS Data Input (0+)	
14	GND	Ground	
15	LV1N1	1st Channel LVDS Data Input (1-)	
16	LV1P1	1st Channel LVDS Data Input (1+)	
17	GND	Ground	
18	LV1N2	1st Channel LVDS Data Input (2-)	
19	LV1P2	1st Channel LVDS Data Input (2+)	
20	GND	Ground	
21	LVCK1N	1st Channel LVDS Clock Input (-)	
22	LVCK1P	1st Channel LVDS Clock Input (+)	
23	GND	Ground	
24	LV1N3	1st Channel LVDS Data Input (3-)	
25	LV1P3	1st Channel LVDS Data Input (3+)	
26	GND	Ground	
27	NC	For CSOT Users Only	(3)
28	NC	For CSOT Users Only	(3)
29	NC	For CSOT Users Only	(3)
30	GND	Ground	

Note:

(1) The direction of pin assignment is shown as below:

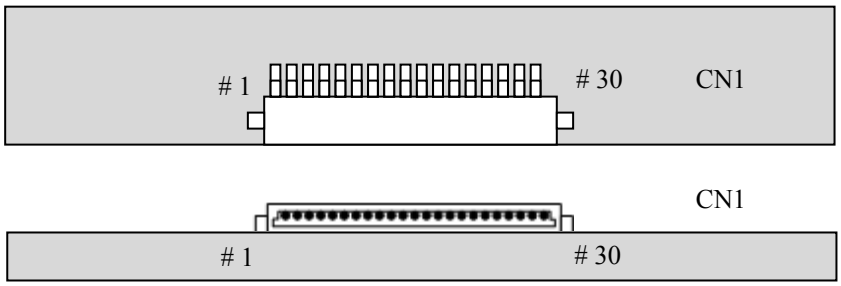
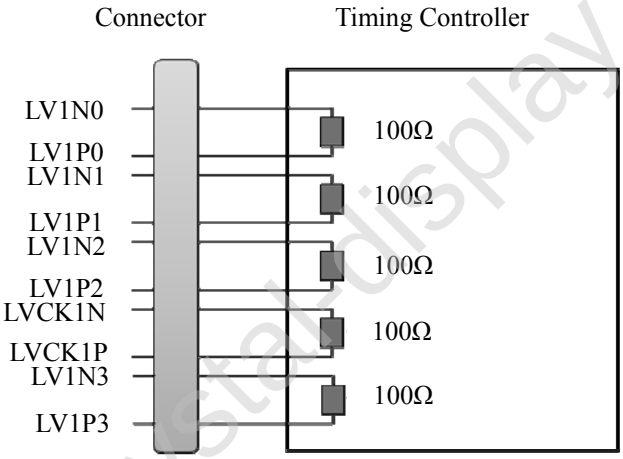


Fig. 3.1 LVDS direction sketch map

(2) High: connect to +3.3 V → JEIDA format; Low: connect to GND or Open → VESA format.

(3) For CSOT internal only, please let it open.

3.2 Block Diagram of Interface



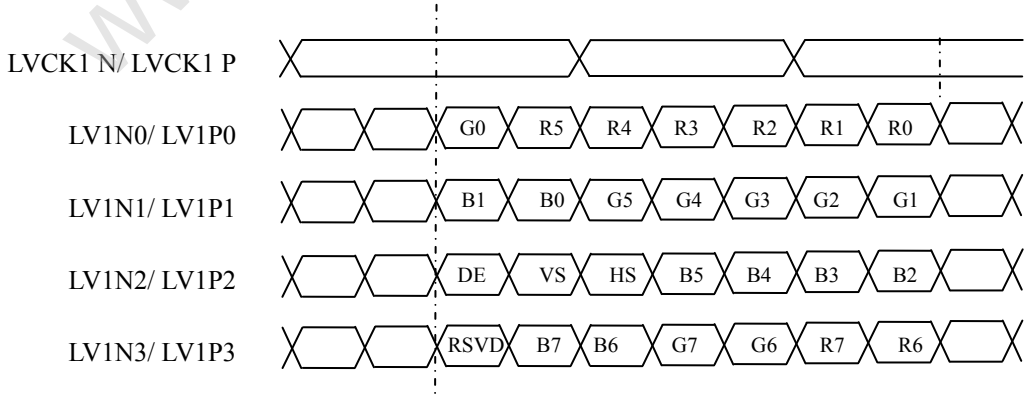
Attention:

(1) This Open cell uses a 100 ohms (Ω) resistor between positive and negative lines of each receiver input.

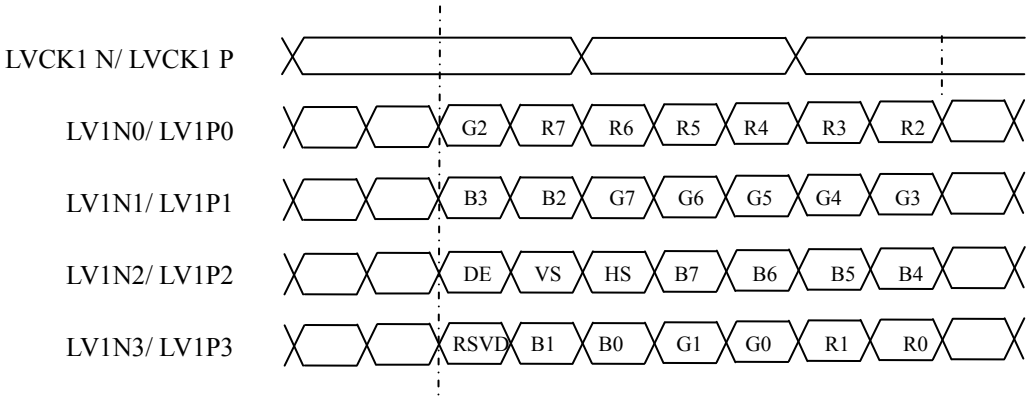
(2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line respectively.

3.3 LVDS Interface

3.3.1 VESA Format (SELLVDS = L or Open)

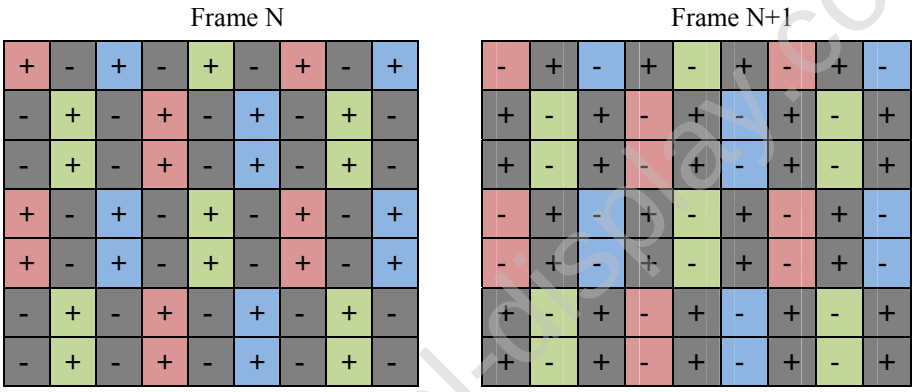


3.3.2 JEIDA Format (SELLVDS = H)



3.4 Pattern FOR Vcom Adjustment

2 line-inversion pattern (2n+1)



4. Interface Timing

4.1 Timing Table (DE Only Mode)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	F_{clk} (= 1 / T_{clk})	50.0	75.4	85.0	MHz	
Vertical Term	Frame Rate	F	57	60	63	Hz	
	Vertical Frequency	F_v	47.0	48.4	60.9	KHz	
	Total	T_v	784	806	1015	T_h	$T_v = T_{vd} + T_{vb}$
	Display	T_{vd}		768			
	Blank	T_{vb}	16	38	247	T_h	
Horizontal Term	Total	T_h	1460	1560	2000	T_{clk}	$T_h = T_{hd} + T_{hb}$
	Display	T_{hd}		1366			
	Blank	T_{hb}	94	194	634	T_{clk}	

Attention:

(1) The TFT LCD Open cell is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.

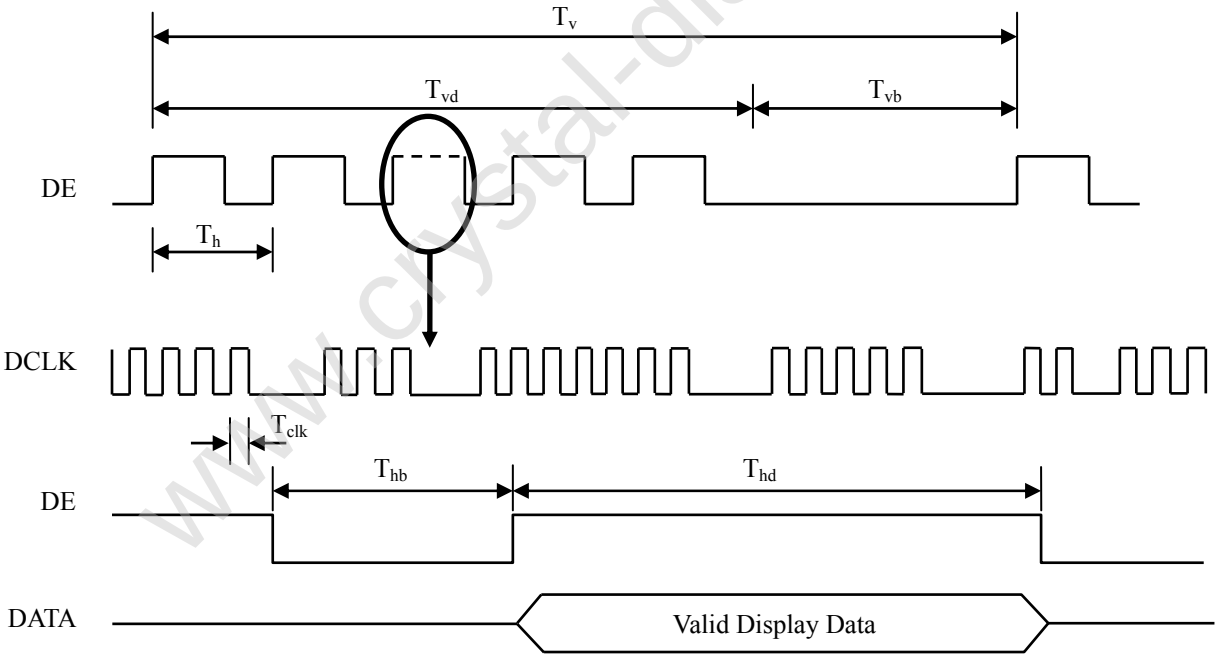


Fig. 4.1 Interface signal timing diagram

4.2 Power On/Off Sequence

To prevent a latch-up or DC operation of the Open cell, the power on/off sequence should be as the diagram below.

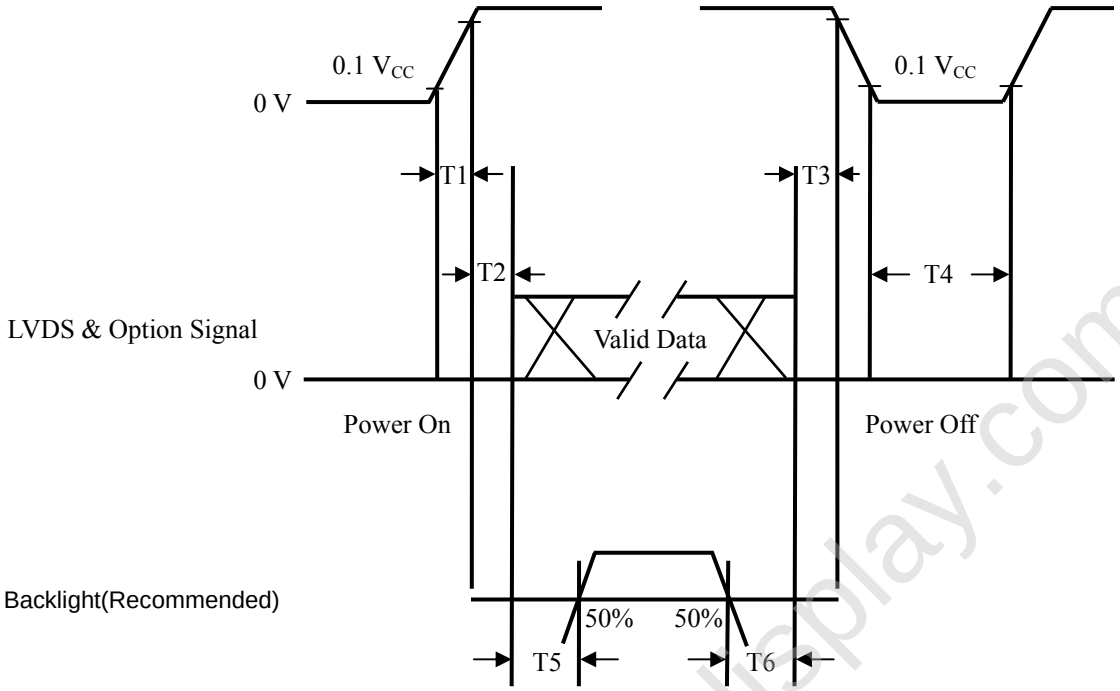


Fig. 4.2 Power On/Off

Parameter	Values			Unit
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	0	-	50	ms
T4	1000	-	-	ms
T5	500	-	-	ms
T6	100	-	-	ms

Attention:

(1) The supply voltage of the external system for the open cell input should follow the definition of V_{CC}.

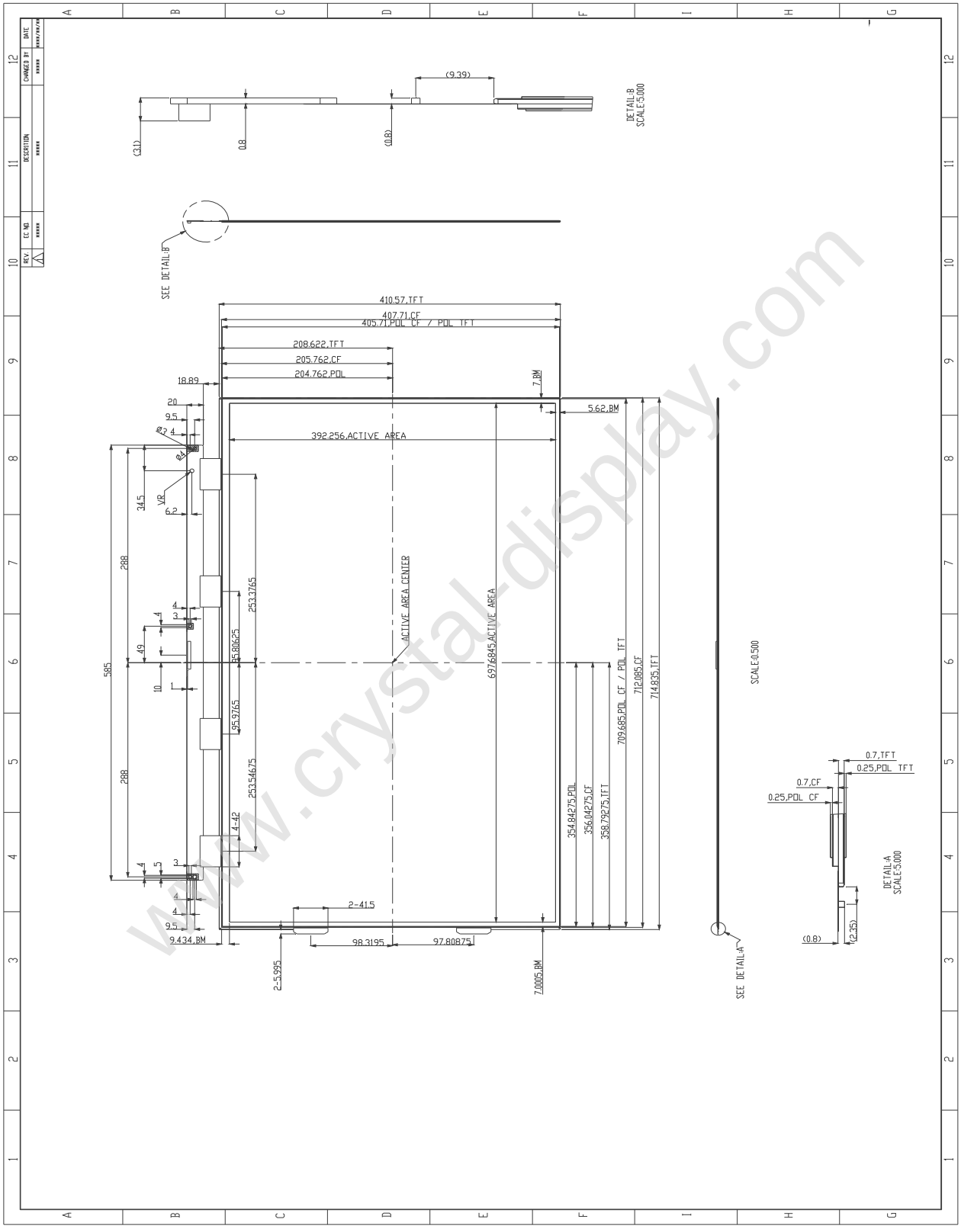
(2) When the customer's backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case that V_{CC} is in off level, please keep the level of input signals on the low or high impedance. If T2 < 0, that may cause electrical overstress.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

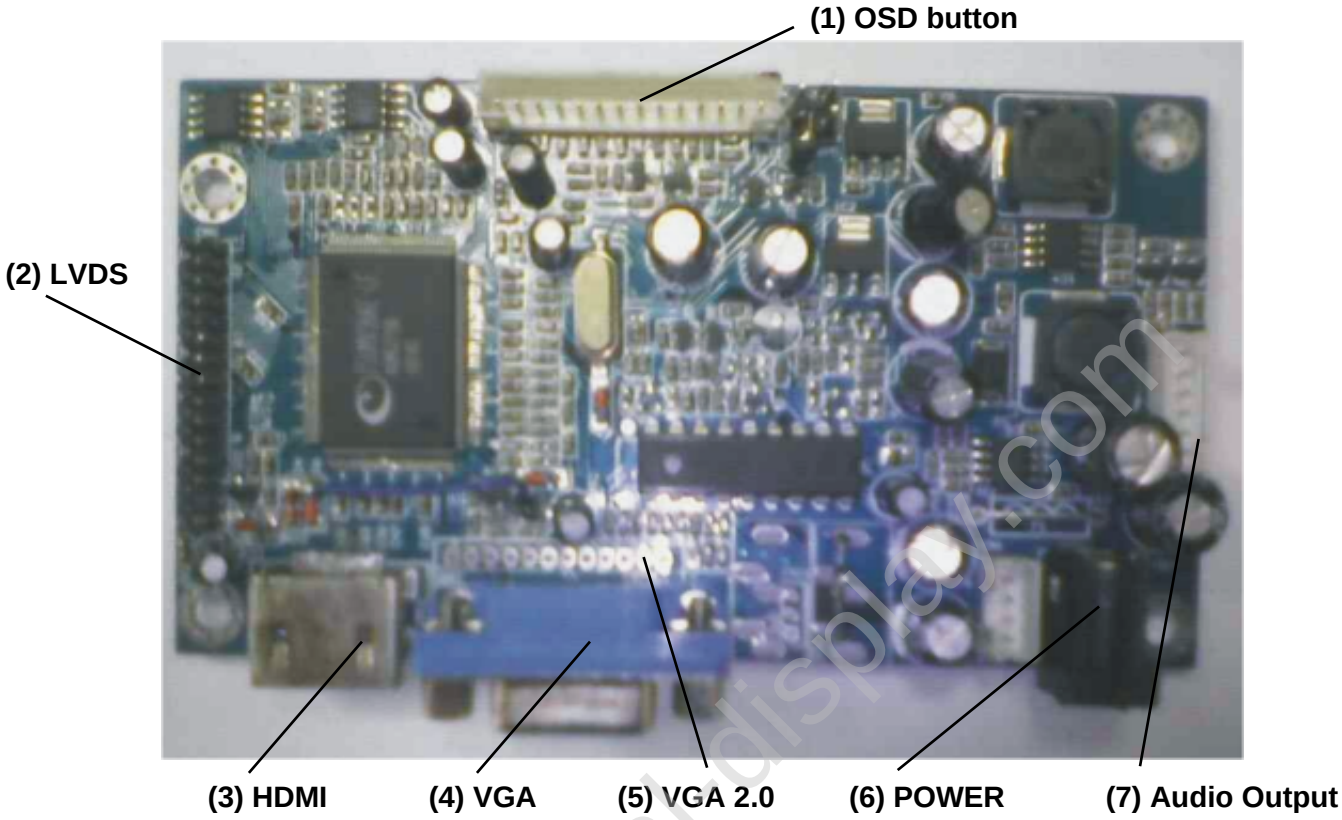
(5) Interface signal shall not be kept at high impedance when the power is on.

5. Panel Mechanical Drawing



6. A/D BOARD

6.1 A/D BOARD SPECIFICATIONS

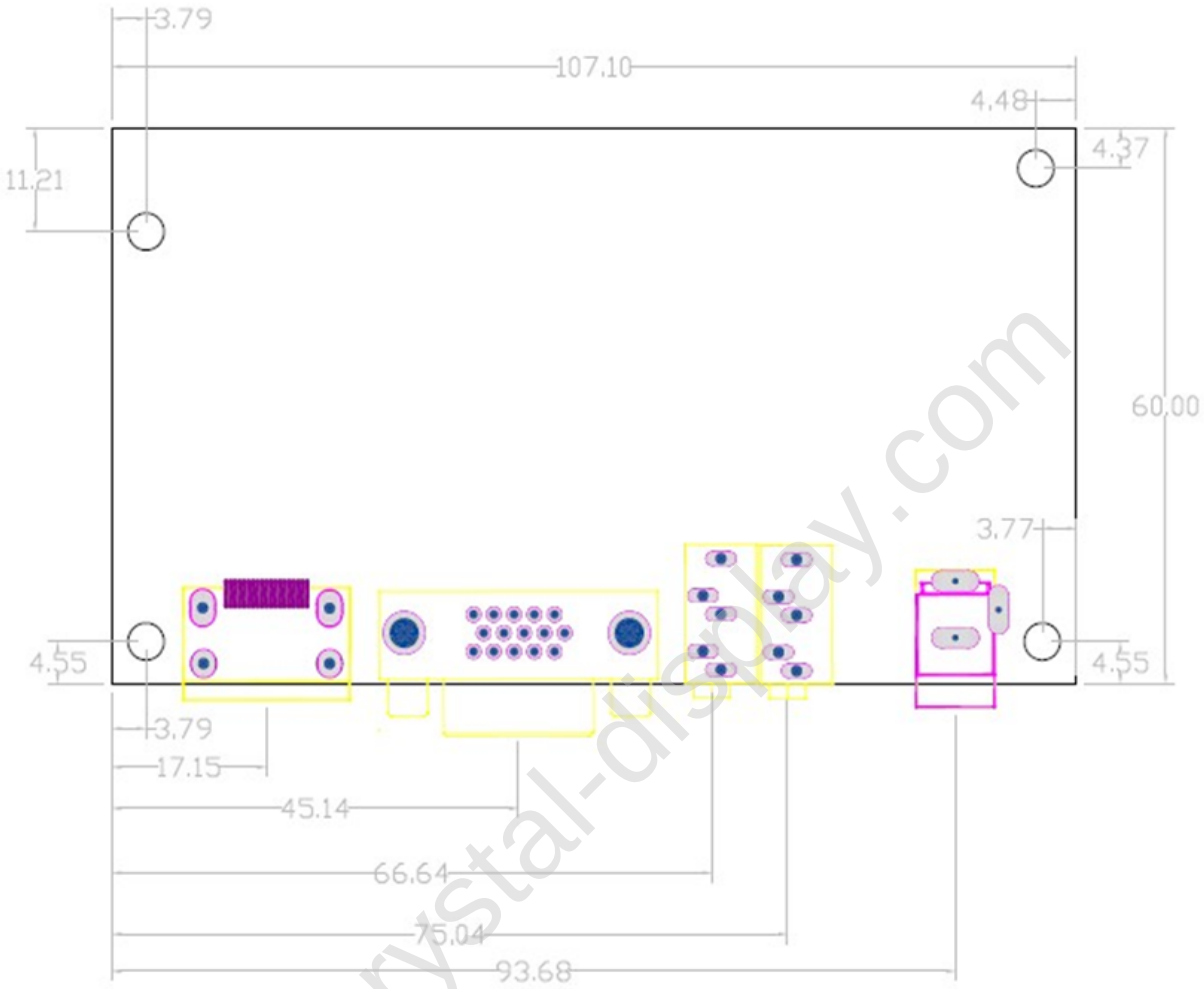


6.2 RESOLUTION SUPPORT

VGA
640x480
800x600
1024x768
1280x1024
1440x900
1600x1200
1600x1050
1920x1080
1920x1200
1280x800
1280x960
1280x720

HDMI	
640x480	720-50Hz
800x600	720-60Hz
1024x768	720-24Hz
1280x1024	720-25Hz
1440x900	720-30Hz
1600x1200	1080i 50
1600x1050	1080i 60
1920x1080	1080p 24
1920x1200	1080p 25
1280x800	1080p 30
1280x960	1080p 50
480i	1080p 60
480p	
576i	
576p	

6.3 A/D BOARD Mechanical Drawing



7. LVDS Cable

LVDS Cable connects the Panel AND A/D Board

LVDS Cable length :40cm